Remarks

This is in response to the Office Action mailed on August 29, 2002. Claims 1 and 4 have been amended, support for which is found at page 6, line 29 - page 7, line 4 of the present application. No new matter has been added. Claims 1-4 remain pending. Reconsideration and allowance are respectfully requested.

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the rejection states that it is unclear whether the recitation of "connecting the power supply line . . . with the ground line" is a process step that is carried out. Claim 1 has been amended to remove the specific recitation of this step, and the arranging step has been amended to recite that the power supply capacitor cells are arranged in the vicinity of the logic gate cells so as to connect the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells. Claim 1 is sufficiently definite to satisfy section 112. Reconsideration and allowance of claim 1 are respectfully requested.

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Uchida, U.S. Patent No. 6,430,735, in view of Sunter et al., U.S. Patent No. 6,204,694. This rejection is respectfully traversed.

Claim 1 is directed to a LSI layout method including steps of: (1) determining a capacitance value of power supply capacitor cells so as to correspond to a drive load capacity value of logic gate cells; and (2) arranging the power supply capacitor cells in a vicinity of the logic gate cells to connect a power supply line of the logic gate with a ground line of the logic gate through the power supply capacitor cells. The method recited in claim 1 is advantageous in that each logic gate cell is driven by power from the power supply capacitor cell to operate more stably, and power supply noise of the LSI circuit can be reduced as well.

The rejection characterizes Uchida as disclosing a method for automatic arranging of blocks in LSI, including placing capacitor blocks in the vicinity of the logic gate cells, as well as in areas not used for other functions. For this response only, this interpretation of Uchida is not disputed. However, as the rejection notes, Uchida fails to disclose the step of determining the capacitance, as recited in claim 1.

Sunter is relied upon for disclosing determination of the capacitance, as well as setting of the capacitance value. This interpretation of Sunter is respectfully traversed. Sunter discloses a circuit that can freely designate its speed by switching a ring oscillator disposed in the circuit. A

capacitor arranged at an output of the ring oscillator is used to adjust a delay amount of a delay circuit. Based on the capacitor value C, capacitor values are set as 4C, 2C, etc. See column 11, lines 56-67 of Sunter. The delay amount is increased as the capacitor value C is increased. Therefore, Sunter is concerned with setting the delay amount based on the capacitor selected. See the abstract of Sunter.

Sunter fails to disclose or suggest determining the capacitance value of power supply capacitor cells so as to correspond to a drive load capacity value of logic gate cells, as recited by claim 1. For at least this reason, the combination of Uchida with Sunter fails to render claim 1, as well as claims 2 and 3 that depend therefrom, obvious.

Claim 4 is also directed to an LSI layout method including steps of: (1) calculating a possible number of power supply capacitor cells to be arranged based on the width of dead space of the power supply and the width of the power supply capacitor cells; and (2) arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged. The method recited in claim 4 provides the advantageous of reducing power supply noise without increasing respective block areas of the LSI. The method may also enable arrangement of a maximum number of capacitors, resulting in stabilization of the power supply of the logic gate and reduction in power supply noise.

Neither cited reference, alone or in combination, recites the limitations of claim 4. Specifically, neither reference suggests calculating the possible number of power supply capacitor cells to be arranged, as recited by claim 4. Therefore, for at least this reason, claim 4 is allowable over the cited art.

In view of the above, favorable reconsideration of claims 1-4 in the form of a Notice of Allowance is requested. The Examiner is invited to telephone the undersigned at (612) 371-5237 with any questions regarding this application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS

In The Claims

Please amend claims 1 and 4 as follows.

1. (Twice Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells,

[connecting the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells,] and

arranging the power supply capacitor cells in [the] a vicinity of the logic gate cells so as to connect a power supply line of the logic gate with a ground line of the logic gate through the power supply cells.

4. (Twice Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

[connecting the power supply line of the logic gate with the ground line of the logic gate through the power supply capacitor cells,]

calculating a possible number of the power supply capacitor cells to be arranged based on a width of a dead space of the power supply and a width of the power supply capacitor cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.